ABSTRACT OF THE DISCLOSURE

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A sense amplifier power-gating circuit and method is disclosed which is of particular utility with respect to DRAM devices, or those incorporating embedded DRAM, and having a power-down (or Sleep) mode 5 of operation. In accordance with a particular technique of the present invention, the local sense amplifier driver transistors serve a dual purpose as both driver and power gate transistors thereby obviating the need for large, distinct power-gating This serves to minimize on-chip area requirements while not degrading sensing speed as in conventional approaches.